WHAT IS CLAIMED IS:

1. A processing apparatus comprising:

a memory capable of storing data;

a butterfly arithmetic unit for performing butterfly computation processes; and

a bit-reversed order shuffle processing unit for writing results obtained by the butterfly computation processes performed by said butterfly arithmetic unit at addresses in said memory after bit-reversed order shuffle instead of writing the results at addresses in said memory in processing order,

wherein data written by said bit-reversed order shuffle processing unit are discrete fast Fourier transform results.

2. The processing apparatus according to claim 1, wherein

said processing apparatus further comprises

a complex conjugate data transforming unit for transforming input real data into complex data, and

an output reconstruction arithmetic unit for reading out the data written in said memory by said bit-reversed order shuffle processing unit and performing an output reconstruction computation process, wherein

said butterfly arithmetic unit performs a butterfly computation process for the complex conjugate data, and

output reconstruction computation process results

obtained by said output reconstruction arithmetic unit are real discrete Fourier transform results.

3. The processing apparatus according to claim 1, wherein

said processing apparatus further comprises an output reconstruction arithmetic unit for performing an output reconstruction computation process, wherein

said butterfly arithmetic unit performs a butterfly computation process for the data having undergone the output reconstruction computation process, and

the data written by said bit-reversed order shuffle processing unit are real inverse discrete Fourier transform results.

4. The processing apparatus according to claim 1, wherein

said butterfly arithmetic unit reads out data from said memory and performs a butterfly computation process, and

said bit-reversed order shuffle processing unit leaves necessary data to be read out from said memory by said butterfly arithmetic unit afterward and overwrites the butterfly computation process results at addresses of unnecessary data that have already been read out.

5. The processing apparatus according to claim 4, wherein said butterfly arithmetic unit controls a read sequence of data from said memory so as to

prevent said bit-reversed order shuffle processing unit from overwriting the necessary data.

6. A processing apparatus comprising:

a butterfly arithmetic unit for performing butterfly computation processes and writing results obtained by the butterfly computation processes in a memory; and

a bit-reversed order shuffle processing unit for reading out the results obtained by the butterfly computation processes and written in the memory from addresses in the memory upon bit-reversed order shuffle,

wherein data read out by said bit-reversed order shuffle processing unit are discrete fast Fourier transform results.

7. The processing apparatus according to claim 6, wherein

said processing apparatus further comprises

a complex conjugate data transforming unit for transforming input real data into complex data, and

an output reconstruction arithmetic unit for performing an output reconstruction computation process for the data read out by said bit-reversed order shuffle processing unit, wherein

said butterfly arithmetic unit performs a butterfly computation process for the complex conjugate data, and

output reconstruction computation process results

obtained by said output reconstruction arithmetic unit are real discrete Fourier transform results.

8. The processing apparatus according to claim 6, wherein

said processing apparatus further comprises an output reconstruction arithmetic unit for performing an output reconstruction computation process, wherein

said butterfly arithmetic unit performs a butterfly computation process for the data having undergone the output reconstruction computation process, and

the data read out by said bit-reversed order shuffle processing unit are real inverse discrete Fourier transform results.

9. The processing apparatus according to claim 6, further comprising a post-processing unit for processing the data read out by said bit-reversed order shuffle processing unit.

10. The processing apparatus according to claim 9, wherein said post-processing unit leaves necessary data to be read out from said memory by said bit-reversed order shuffle processing unit afterward and overwrites process results at addresses of unnecessary data that have already been read out.

11. The processing apparatus according to 10, wherein said bit-reversed order shuffle processing unit controls a read sequence of data from said memory so as to prevent said post-processing unit

from overwriting the necessary data.

12. A processing apparatus for executing a sequence of reading out data one by one from an external unit or a memory, performing a series of computation processes including a discrete fast Fourier transform process for the data, and writing the data in the memory, as one unit, with respect to all the data sequentially and repeatedly under pipeline sequence control adjusted to inhibit concurrent execution of computations of the same type, thereby processing one computation process group, and deriving computation results by continuously executing the series of computation processes, comprising:

an arithmetic unit for executing a computation of input data; and

a memory for storing a computation result obtained by said arithmetic unit,

wherein said arithmetic unit has a process latency until the input data is input and processed and the process result is output, the process latency being a time adjusted to inhibit data in the memory which is required for a subsequent computation process during a computation process from being overwritten by output data, and

a bit-reversed order shuffle process group and an immediately preceding or succeeding process group can be processed in a sequence as one unit by said

arithmetic unit having the process latency.

13. The processing apparatus according to claim 12, wherein a bit-reversed order shuffle process group of a discrete fast Fourier transform process and an immediately preceding butterfly computation process group can be processed in a sequence as one unit.

14. The processing apparatus according to claim 13, wherein a real discrete Fourier transform is performed.

15. The processing apparatus according to claim 13, wherein a real inverse discrete Fourier transform is performed.

16. The processing apparatus according to claim 12, wherein a bit-reversed order shuffle process group of a real discrete Fourier transform process and an immediately succeeding output reconstruction computation process group can be processed in a sequence as one unit.

17. A processing method comprising:

a butterfly computation process step of performing butterfly computation processes; and

a bit-reversed order shuffle process step of writing results obtained by the butterfly computation processes at addresses in a memory upon bit-reversed order shuffle instead of writing the results at addresses in the memory in processing order,

wherein data written in the bit-reversed order

shuffle process step are discrete fast Fourier transform results.

18. A processing method comprising:

a butterfly computation process step of performing butterfly computation processes and writing results obtained by the butterfly computation processes in a memory; and

a bit-reversed order shuffle process step of reading out the results obtained by the butterfly computation processes and written in the memory from addresses in the memory upon bit-reversed order shuffle,

wherein data read out in the bit-reversed order shuffle process step are discrete fast Fourier transform results.

19. A program for causing a computer to execute:

a butterfly computation process step of performing butterfly computation processes; and

a bit-reversed order shuffle process step of writing results obtained by the butterfly computation processes at addresses in a memory upon bit-reversed order shuffle instead of writing the results at addresses in the memory in processing order.

20. A program for causing a computer to execute:

a butterfly computation process step of performing butterfly computation processes and writing results obtained by the butterfly computation processes in a memory; and

a bit-reversed order shuffle process step of reading out the results obtained by the butterfly computation processes and written in the memory from addresses in the memory upon bit-reversed order shuffle.